CLAIMS:

1. (Currently Amended): An apparatus for performing commands, comprising:

performance logic, wherein the performance logic is at least configured to perform a plurality of commands issued by a processor, and wherein the performance logic further comprises a command queue [[with]] having a queue depth equal to a predefined number of slots for storing the plurality of commands issued by the processor;

a command pipeline, wherein the command pipeline at least communicates the plurality of commands issued by the processor to the performance logic;

a plurality of counters, wherein a known counter within the plurality of counters at least determine represents a known count of a number of commands in the command pipeline and in the command queue, and wherein an unknown counter within the plurality of counters at least predicts an represents a predicted unknown count of future commands; and

stall logic, wherein the stall logic at least has the ability to stall stalls performance of the plurality of commands issued by the processor based on at least a use of the unknown count and the known count responsive to a sum of the known counter and the unknown counter being greater than the queue depth.

2. (Currently Amended): The apparatus of Claim 1, wherein the performing logic further comprises:

fetch logic, wherein the fetch logic at least retrieves the plurality of commands from the command pipeline to at least provide a plurality of fetched command;

decode logic, wherein the decode logic at least decodes the plurality of fetched command to at least provide a plurality of decoded commands;

issue logic, wherein the issue logic at least issues the plurality of decoded commands to the command queue of the performance logic; and

execution logic to execute the plurality of decoded command in the command queue.

3. (Canceled)

4. (Canceled)

5. (Currently Amended): The apparatus of Claim 1 wherein the stall logic further comprises:

 a tracking pipeline, wherein the tracking pipeline monitors progress of the plurality of commands and stall requests to at least provide a control signal;

 an incrementer, wherein the incrementer increments the unknown count counter based on the control signal responsive to a stall being issued; and

 a decrementer, wherein the decrementer decrements the unknown count counter based on the control signal responsive to a stall being completed.

6-11. (Canceled)

12. (Currently Amended): [[The]] A method of stalling performance of commands in a command performance system, comprising:

 executing a plurality of commands;

 reporting command progress of the plurality of commands to stall logic during execution;

 determining if the performance misses during execution;

 if the performance misses, storing the command in a command queue; [[and]]

 determining a known count of a number of commands in a command pipeline and in a command queue;

 determining an unknown count prediction of future commands;

 determining a sum of the known count and the unknown count;

 determining if the sum is greater than a predefined number of slots in the command queue; and

 if the sum is greater than a predefined number of slots in the command queue, stalling the command performance based on misses and progress of the plurality of commands.

13. (Original): The method of Claim 12, where the step of stalling the command performance further comprises receiving a completion signal when stored commands are performed.

14-19. (Canceled)

20. (New): The method of Claim 12, further comprising:
    incrementing the unknown counter responsive to a stall being issued.

21. (New): The method of Claim 12, further comprising:
    decrementing the unknown counter responsive to a stall being completed.

22. (New): An apparatus for stalling performance of commands in a command performance system, comprising:
    means for executing a plurality of commands;
    means for reporting command progress of the plurality of commands to stall logic during execution;
    means for determining if the performance misses during execution;
    means for storing the command in a command queue if the performance misses;
    means for determining a known count of a number of commands in a command pipeline and in a command queue;
    means for determining an unknown count prediction of future commands;
    means for determining a sum of the known count and the unknown count;
    means for determining if the sum is greater than a predefined number of slots in the command queue; and
    means for stalling the command performance based on misses and progress of the plurality of commands if the sum is greater than a predefined number of slots in the command queue.

23. (New): The apparatus of Claim 22, wherein the means for stalling further comprises:
    means for monitoring progress of the plurality of commands and stall requests;

means for incrementing the unknown counter responsive to a stall being issued; and

means for decrementing the unknown counter responsive to a stall being completed.

24. (New): The apparatus of Claim 22, where the means for stalling the command performance further comprises means for receiving a completion signal when stored commands are performed.

25. (New): The apparatus of Claim 22, further comprising:

means for incrementing the unknown counter responsive to a stall being issued.

26. (New): The apparatus of Claim 22, further comprising:

means for decrementing the unknown counter responsive to a stall being completed.